1. (*Amended*) A semiconductor device comprising:

B1

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,

Sub C1

a contact portion for applying to the semiconductor substrate different bias voltages in an operating state and a standby state of a semiconductor circuit including the MOS transistor,

the transistor including source and drain regions of a second conductivity type, a channel of the first conductivity type, and wherein an impurity diffusion layer of the first conductivity type is formed in the semiconductor substrate under at least the entire source, drain and channel regions, so that the impurity diffusion layer is of the same conductivity type as the semiconductor substrate,

wherein the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias voltages are applied to the substrate via the impurity diffusion layer; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltage for both of the transistors is changed between the active and standby states so that active regions of the transistors are fully depleted simultaneously in the standby state.

B2

4. (*Amended*) A semiconductor device according to claim 1, wherein the impurity diffusion region is formed as a well in a surface of the semiconductor substrate which lies under the first MOS transistor, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

B3

Sub C2

5. (*Amended*) A semiconductor device according to claim 4, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said MOS transistors, while a well for the other of the MOS transistors is an N-type well under a P-channel MOS transistor which is the second of said MOS transistors.

B4

6. (*Amended*) A semiconductor device according to claim 5, wherein a plurality of wells including the P-type well and the N-type well are formed in the semiconductor substrate and the P-type well and the N-type well are substantially electrically isolated from each other.

Sub C3

7. (*Amended*) A semiconductor device comprising:

a first MOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate with the intervention of a buried insulating film,

an element isolating region formed in the semiconductor layer,

a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the semiconductor substrate, the

well being of the first conductivity type as is the other region of the semiconductor substrate directly under the well; and

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the substrate, and wherein bias voltage for both of the transistors is changed between the active and standby states so that active regions of the transistors are fully depleted simultaneously in the standby state.

8. (*Amended*) A semiconductor device according to claim 7, wherein the well is formed in a surface of the semiconductor substrate which lies under the first MOS transistor formed on the semiconductor layer, the well having an impurity concentration higher than that of the other region of the substrate, and the bias voltages are applied to the well.

9. (*Amended*) A semiconductor device according to claim 8, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said MOS transistors, while a well for the other of the MOS transistors is an N-type well under a P-channel MOS transistor which is the second of said MOS transistors.

24. (*Amended*) A semiconductor device comprising:

a PMOS transistor and an NMOS transistor formed on a semiconductor layer of an SOI substrate in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,